UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/898,321	07/02/2001	Robert A. Street	A0682	4769

28014 7590 04/01/2003

BEVER, HOFFMAN & HARMS, LLP
2099 GATEWAY PLACE
SUITE 320
SAN JOSE, CA 95110

EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/898,321	STREET ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 21-30* is/are pending in the application.

4a) Of the above claim(s) *22 and 23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,21 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *10 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Newly submitted claims 22, 23 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Invention I, claims 1 – 10, 21, and 24 – 30, recite an integrated circuit structure having an air gap structure defined at crossover locations of gate lines and data lines. Invention II, claims 22 and 23, recite an integrated circuit structure with an optical filter island over a first region in combination with the air gap structure defined at crossover locations of gate lines and data lines.

Inventions II and I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of an air gap structure of the subcombination as claimed for patentability because an air gap structure of the combination claims does not require support structures. The subcombination has separate utility such as in a device without an optical filter.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 22 and 23 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 24, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 27 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 27 recites the limitation "the first metal layer" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action "formed from the first metal layer" will be omitted.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 – 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kingsley et al. (USPAT 5587591) in view of Ahn (USPAT 6037248).

With regard to claim 1, Kingsley discloses in figures 1b – 2b an integrated circuit. Kingsley discloses in figures 1b – 2b a plurality of pixel circuits (134) arranged in rows and columns. Kingsley discloses in figures 1b – 2b a plurality of first lines (132), each first line connected to a corresponding column of pixel circuits. Kingsley discloses in figures 1b – 2b a plurality of second lines (131), each second line connected to a corresponding row of pixel circuits. Kingsley discloses in figure 2b wherein the plurality of first lines are formed such that each first line extends over the plurality of second lines at corresponding crossover locations. Kingsley discloses in figure 2a where an insulator is defined at each crossover location that separates each first line from the plurality of second lines. Kingsley does not disclose that the insulator is an air-gap. Ahn teaches in figure 10 wherein an air-gap (56) is defined at each crossover location that separates a first line (70) from a plurality of second lines (36), wherein each air gap extends from a top surface of a corresponding second line to a bottom surface of the each first line. It would have been obvious to one of ordinary skill in the art at the time of the

present invention to use the air gap of Ahn in the device of Kingsley in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

With regard to claim 2, Kingsley discloses in figures 1b – 2b wherein each pixel circuit includes an access transistor (134) and a pixel element (120), wherein the access transistor includes a gate terminal connected (136) to an associated first line, a first terminal (137) connected to the pixel element, and a second terminal (138) connected to an associated second line.

With regard to claim 3, Kingsley discloses in figures 1b – 2b, column 4, lines 57 – 67 and column 5, lines 1 – 3 wherein the access transistor comprises amorphous silicon.

With regard to claim 6, Kingsley discloses in column 1, lines 9 – 16 wherein the integrated circuit comprises a medical image sensor array.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kingsley and Ahn as applied to claims 1 and 2 above, and further in view of Akiyama et al. (USPAT 5712494, Akiyama).

With regard to claim 4, it is not clear if Kingsley and Ahn disclose wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor. Akiyama teaches in figures 1a – 1d wherein an access transistor of an each pixel circuit comprises a self-aligned thin-film transistor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the self-aligned thin-film transistor of Akiyama in the device of Kingsley and Ahn in order to use a thin film field effect transistor which can be operated at high speed even if a channel length is shortened.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kingsley and Ahn as applied to claims 1 and 2 above, and further in view of Hwang et al. (USPAT 6337284, Hwang).

With regard to claim 5, Kingsley and Ahn do not teach wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated second line by a buried insulator layer comprising a resin derived from 2-staged bisbenzocyclobutene monomers. Hwang teaches in figures 1 – 2d and column 2, lines 15 – 24 wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated second line by a buried insulator layer comprising a resin derived from 2-staged bisbenzocyclobutene monomers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bisbenzocyclobutene of Hwang in the device of Kingsley and Ahn in order to take advantage of the high dielectric constant, high moisture resistance and high resistance to electrical breakdown of bisbenzocyclobutene.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kingsley and Ahn as applied to claims 1 and 2 above, and further in view of Street (USPAT 5789737).

With regard to claim 7, Kingsley discloses in column 3, lines 62 – 67 wherein each pixel element comprises an amorphous silicon sensor. Kingsley and Ahn do not teach wherein each pixel circuit further comprises a phosphor converter located over the amorphous silicon sensor. Street teaches in column 1, lines 11 – 27 wherein each pixel element comprises an amorphous silicon sensor, and wherein each pixel circuit further comprises a phosphor converter located

over the amorphous silicon sensor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the phosphor converter of Street in the device of Kingsley and Ahn in order to convert incoming x-rays to light rays.

11. Claims 8 and 27 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda et al. (USPAT 5623161, Fukuda) in view of Ahn.

With regard to claim 8, Fukuda discloses in figures 1 and 2 an image sensor array. Fukuda discloses in figures 1 and 2 and column 4, lines 57 – 67 a plurality of pixel circuits arranged in rows and columns, each pixel circuit including an access transistor (1). Fukuda discloses in figures 1 and 2 a plurality of gate lines (10), each gate line connected (9) to the access transistors of a corresponding column of pixel circuits. Fukuda discloses in figures 1 and 2 a plurality of data lines (12), each data line connected (11) to the access transistors of a corresponding row of pixel circuits. Fukuda discloses in figures 1 and 2 wherein the plurality of data lines are formed such that each data line overlaps the plurality of gate lines at corresponding crossover locations. Fukuda discloses in figures 1 and 2 where an insulator (3) is defined at each crossover location that separates each data line from the plurality of gate lines. Fukuda does not disclose that the insulator is an air-gap. Ahn teaches in figure 10 wherein an air-gap (56) is defined at each crossover location that separates a data line (70) from the plurality of gate lines (36), wherein each air gap extends from a top surface of a corresponding gate line to a bottom surface of the each data line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Fukuda in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

With regard to claim 27, Fukuda discloses in figures 1 and 2 wherein the image sensor array further comprises spaced apart data line support pads (portions of insulator 3 to the left and right of gate line 10), and wherein each spaced-apart data line support pad contacts an associated data line.

With regard to claim 28, Fukuda discloses in figures 1 and 2 an image sensor array. Fukuda discloses in figures 1 and 2 a substrate having an upper surface defining a plane. Fukuda discloses in figures 1 and 2 a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate. Fukuda discloses in figures 1 and 2 a plurality of first lines, each first line being formed on the upper surface of the substrate and connected to a corresponding first group of said pixel circuits. Fukuda discloses in figures 1 and 2 a plurality of second lines connected to a corresponding second group of said pixel circuits. Fukuda discloses in figures 1 and 2 first portions supported by the upper surface of the substrate. Fukuda discloses in figures 1 and 2 second portions extending over the plurality of first lines at corresponding crossover locations. Fukuda is silent to air gaps. Ahn teaches in figure 10 second portions extending over a plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Fukuda in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

With regard to claim 29, Fukuda discloses in figures 1 and 2 further comprising a plurality of support pads. Fukuda discloses in figures 1 and 2 each support pad being formed on

the upper surface of the substrate and contacting a corresponding first portion of an associated second line.

With regard to claim 30, Fukuda discloses in figures 1 and 2 an image sensor array. Fukuda discloses in figures 1 and 2 a substrate having an upper surface defining a plane. Fukuda discloses in figures 1 and 2 a plurality of pixel circuits arranged in rows and columns over the upper surface of the substrate. Fukuda discloses in figures 1 and 2 a plurality of first lines, each first line being formed over the upper surface of the substrate and connected to a corresponding first group of said pixel circuits. Fukuda discloses in figures 1 and 2 a plurality of support pads, each support pad being formed over the upper surface of the substrate; and a plurality of second lines connected to a corresponding second group of said pixel circuits. Fukuda discloses in figures 1 and 2 a plurality of first portions, each first portion contacting a corresponding support pad. Fukuda discloses in figures 1 and 2 second portions extending between adjacent first portions. Fukuda is silent to air gaps. Ahn teaches in figure 10 second portions extending between adjacent first portions such that each second portion is freely supported by an associated pair of adjacent first portions, wherein each second portion extends over a corresponding first line such that an air gap is defined between the corresponding first line and said each second portion. over a plurality of first lines at corresponding crossover locations such that an air gap is defined at each said crossover location between a top surface of a corresponding first line and a bottom surface of the corresponding second portion of said each second line. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the air gap of Ahn in the device of Fukuda in order to reduce the capacitance between the lines as taught by Ahn in column 3, lines 23 – 26.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda and Ahn as applied to claim 8 above, and further in view of Antonuk et al. (USPAT 5262649, Antonuk).

With regard to claim 9, Fukuda discloses in figures 1 and 2 and column 5, lines 59 – 62 wherein the plurality of gate lines are formed from a first metal layer. Fukuda discloses in figures 1 and 2 and column 6, lines 41 – 50 the plurality of data lines are formed from a second metal layer such that the data lines are located above the first metal layer. Fukuda and Ahn do not disclose what materials comprise a sensor. Antonuk teaches in figures 1 and 2 and column 9, lines 51 – 59 wherein each of a plurality of pixel circuits (50) also comprises a sensor including an amorphous silicon layer (30) formed on a metal plate (22), and wherein the metal plate is formed from a third metal layer formed after a first (14) and second (54) metal layers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the sensor and metal plate of Antonuk in the device of Fukuda and Ahn in order to use a sensor that will achieve real-time diagnostic x-ray radiographic images with immediate presentation after the irradiation without the need to wait for film development or laser scanning of a photostimulable phosphor plate as taught by Antonuk in column 6, lines 18 – 22. It should be noted that "a third metal layer formed after the first and second metal layers" is a product by process limitation which bears no patentable weight in a device claim.

13. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda and Ahn as applied to claim 8 above, and further in view of Kunikiyo (USPUB 2002/0135041).

With regard to claim 10, Fukuda and Ahn are silent to a strengthening insulator formed on the plurality of data lines at the crossover locations. Kunikiyo teaches in figures 12 and 13 further comprising a strengthening insulator (58) formed on the plurality of data lines at the crossover locations. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the strengthening insulator of Kunikiyo in the device of Fukuda and Ahn in order to insulate the data line from structures formed thereon.

14. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda and Ahn as applied to claim 8 above, and further in view of Akiyama.

With regard to claim 21, it is not clear if Fukuda and Ahn teach wherein the access transistor of each pixel circuit comprises a self-aligned thin-film transistor. Akiyama teaches in figures 1a – 1d wherein an access transistor of an each pixel circuit comprises a self-aligned thin-film transistor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the self-aligned thin-film transistor of Akiyama in the device of Fukuda and Ahn in order to use a thin film field effect transistor which can be operated at high speed even if a channel length is shortened.

15. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda and Ahn as applied to claim 8 above, and further in view of Hwang.

With regard to claim 24, Fukuda and Ahn do not teach wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated data line by a buried insulator layer comprising a resin derived from 2-staged bisbenzocyclobutene

monomers. Hwang teaches in figures 1 – 2d and column 2, lines 15 – 24 wherein each of the plurality of pixel circuits also comprises a charge sensing region that is separated from the associated data line by a buried insulator layer comprising a resin derived from 2-staged bisbenzocyclobutene monomers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the bisbenzocyclobutene of Hwang in the device of Fukuda and Ahn in order to take advantage of the high dielectric constant, high moisture resistance and high resistance to electrical breakdown of bisbenzocyclobutene.

16. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda, Ahn, and Hwang as applied to claims 8 and 24 above, and further in view of Pedder (USPAT 5604658).

With regard to claim 25, Fukuda, Ahn, and Hwang are silent to the buried insulator layer has a thickness of 3 to 5 microns. Pedder teaches in column 2, line 1 wherein a buried insulator layer has a thickness of 5 microns. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Pedder in the device of Fukuda, Ahn, and Hwang in order to have a thickness that is well known as an insulating thickness.

17. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda, Ahn, and Hwang as applied to claims 8 and 24 above, and further in view of Kingsley.

With regard to claim 26, Fukuda, Ahn, and Hwang do not teach wherein the charge sensing region of each of the plurality of pixel circuits comprises an amorphous silicon (a-Si:H) layer. Kingsley discloses in column 3, lines 62 – 67 wherein a charge sensing region of each of a plurality of pixel circuits comprises an amorphous silicon (a-Si:H) layer. It would have been

obvious to one of ordinary skill in the art at the time of the present invention to use the amorphous silicon region of Kingsley in the device of Fukuda, Ahn, and Hwang in order to use a sensing means well known in the art.

Response to Arguments

18. Applicant's arguments with respect to claims 1 – 10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 26, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800